UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,952	02/11/2002	Zhong-Hua Li	ATECP005/SNG-024A	6975

32986 7590 12/21/2004

IPSG, P.C.
P.O. BOX 700640
SAN JOSE, CA 95170-0640

EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,952	LI ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 May 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are presented for examination.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

Drawings

3. Figure 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because number and reference characters not plain and legible in figures 1-7, and the drawings figures 3 and 6 are too dark. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Murphy (Murphy), U.S. patent no. 5,128,970.

As per claim 1, AAPA discloses an integrated circuit configured to capture an input signal to produce an output signal, said input signal being synchronized with a first clock signal, said output signal being synchronized with a second clock signal having a second frequency different from a first frequency associated with said first signal, comprising [fig. 3, page 4, lines 9-15]:

a first clock domain gating circuit having a first output terminal and a first input terminal, said first clock domain gating circuit being configured to be clocked by said first clock, said first input terminal being coupled to receive said input signal [fig. 3; page 4, lines 9-24], and

a second clock domain gating circuit having a second output terminal and a second input terminal, said second clock domain circuit being clocked by said second clock, said second input terminal being coupled to said first output terminal to receive said latched output [fig. 3; page 5, line 1-page 6, line 2].

AAPA does not explicitly disclose that first clock domain gating circuit being configured to toggle a state of a signal on said first output terminal from one of a first

state and a second state to the other of said first state and said second state every time a pulse is detected in said input signal, thereby producing a latched output at said first output terminal. In other words, AAPA fails to disclose a logic circuit to perform such function indicated above. Also, AAPA does not explicitly disclose that second clock domain gating circuit being configured to produce a pulse on said output signal at said second output terminal, said pulse on said output signal having a duration at least as long as a period of said second clock every time a state of said latched output changes. In other words, AAPA also fails to disclose a logic circuit to perform such function indicated above.

However, Murphy discloses that a logic circuit [100, 102, 106, fig. 2] to perform said first clock domain gating circuit being configured to toggle a state of a signal on said first output terminal from one of a first state and a second state to the other of said first state and said second state every time a pulse is detected in said input signal, thereby producing a latched output at said first output terminal [col. 3, lines 63-68; col. 4, lines 7-25]; and Murphy also discloses that another logic circuit [26, 28, 30, fig. 1a] to perform said second clock domain gating circuit being configured to produce a pulse on said output signal at said second output terminal, said pulse on said output signal having a duration at least as long as a period of said second clock every time a state of said latched output changes [col. 2, lines 14-20, 44-50].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of AAPA and Murphy because they are both directed to a synchronizer circuit system, and the specify teachings of Murphy stated above would

provide an reliable means of efficiency for synchronizing clock signals of AAPA's system.

As per claim 2, Murphy discloses that first clock domain gating circuit includes a first D flip-flop, said first input terminal being coupled to an ENABLE input of said first D flip-flop, said first output terminal being coupled to a first output terminal of said first D flip-flop, said first D flip-flop further includes a first complementary output terminal and a first data input terminal, said first complementary output terminal being coupled to said first data input terminal [fig. 2; col. 3, lines 63-68; col. 4, lines 7-25].

As to claims 3 and 5, Murphy discloses that second clock domain gating circuit includes a plurality of cascaded D flip-flops and an XOR gate [30, 52], wherein said second input terminal representing a data input terminal of one of said plurality of cascaded D flip-flops, an output of a next-to-last cascaded D flip-flop plurality of cascaded D flip-flops being coupled to a first input of said XOR gate, an output of a last-cascaded D flip-flop of said plurality of cascaded D flip-flops to a second input of said XOR gate, wherein said second output terminal of said second clock domain gating circuit is coupled to an output terminal of said XOR gate [figures 1a, 1b; col. 2, lines 14-20, 44-50].

As to claims 4 and 6, AAPA discloses that second frequency is slower than said first frequency [page 4, lines 10-11].

As to claims 7-21, claims 1-6 basically are the corresponding elements that are carried out the method of operating steps in claims 7-21. Accordingly, claims 7-21 are rejected for the same reason as set forth for claims 1-6.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakura et al., US patent no. 6,249,157, discloses a synchronize circuit for to performing said first clock domain gating circuit being configured to toggle a state of a signal on said first output terminal from one of a first state and a second state to the other of said first state and said second state every time a pulse is detected in said input signal, thereby producing a latched output at said first output terminal [figures 1, 25; col. 3, lines 63-67].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

Dec. 16, 2004